CS 362 Architecture **Fall 2025**

http://neilklingensmith.com/teaching/loyola/cs362-f2025

Homework 3

Due: September 4, 2024

Name:

1. (15 points) A multiplexor is a logic device that selects between one of two inputs (**A** or **B**). If `S = 0`, the output of the multiplexor equals `A`. If `S = 1`, the output of the multiplexor equals `B`.

S	A	B	Out
0	**0**	**0**	0
0	**0**	**1**	0
0	**1**	**0**	1
0	**1**	**1**	1
1	**0**	**0**	0
1	**0**	**1**	1
1	**1**	**0**	0
1	**1**	**1**	1

   It is possible to have a 4-input multiplexor that selects between one of four inputs `A`, `B`, `C`, or `D` using a 2-bit select signal `S1 S2`.

   (a) (5 points) Write a truth table for the 4-to-1 multiplexor.

   (b) (10 points) Design logic gate implementation of the 4-to-1 multiplexor based on your truth table. You can use either a Karnaugh map, sum-of-products, or old school Boolean Algebra to implement your design in gates. Use whatever gates you want (AND, OR, NOT, etc). Show your work.

2. (5 points) In this question, you're going to design a shifter that shifts a four bit number right by an arbitrary number of bits. For each bit of the output, use a 4-to-1 multiplexor to select which bit of the input is selected.

3. (10 points) Ethernet frames start with a 7-byte preamble of alternating 1's and 0's (7 bytes of `0xAA`) followed by 1 byte of `0xAD` (called the start-of-frame delimeter).

   Design a state machine that recognizes the bit pattern `101010101011` (a truncated version of the preamble plus the start-of-frame delimiter).

   Hint: you can use a classical state diagram approach or use a shift register.