CS 362 Architecture **Fall 2024**

http://neilklingensmith.com/teaching/loyola/cs362-f2024

Homework 1

Due: September 4, 2024

Name:

1. (25 points) I have compiled a C program into assembly code below. The C function implements the `rot13` encryption/decryption algorithm. Assume every instruction takes one cycle.

```
void rot13(char *text) {
    int i = 0;
    while (text[i]) {
        text[i++] = (((text[i] - 'a') + 13) % 26) + 'a';
    }
}
```

```
; i386 Variant
rot13:
        pushl        %ebx
        movl        8(%esp), %ecx
        movsbl        (%ecx), %eax
        testb        %al, %al
        je         .L1
        movl        $26, %ebx
.L3:
        subl        $84, %eax
        cltd
        idivl        %ebx
        addl        $97, %edx
        movb        %dl, (%ecx)
        incl        %ecx
        movsbl        (%ecx), %eax
        testb        %al, %al
        jne        .L3
.L1:
        popl        %ebx
        ret
```

```
; RISC-V Variant
rot13:
        lbu        a5,0(a0)
        beq        a5,zero,.L1
        li        a4,26
.L3:
        addi        a5,a5,-84
        rem        a5,a5,a4
        addi        a0,a0,1
        addi        a5,a5,97
        sb        a5,-1(a0)
        lbu        a5,0(a0)
        bne        a5,zero,.L3
.L1:
        ret
```

(a) (5 points) How many cycles does the **inner loop** of the x86 variant take?

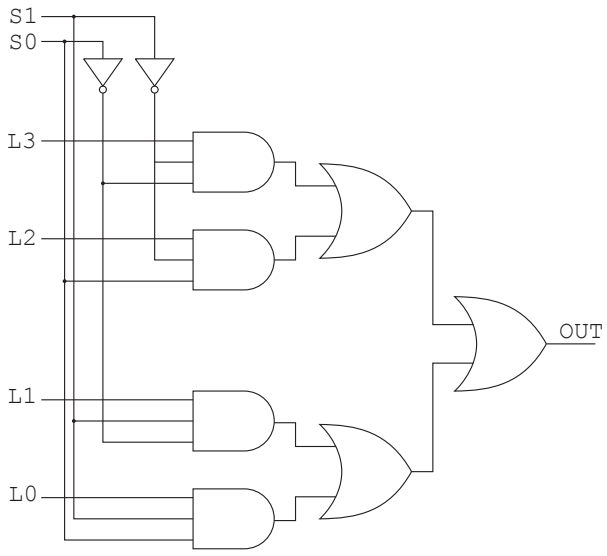
(b) (5 points) How many cycles does the **inner loop** of the RISC-V variant take?

(c) (5 points) If we run the x86 code on a 1GHz x86 CPU with an input string of 10,000 characters, what is the total runtime for the **inner loop**?

(d) (5 points) If we run the RISC-V code on a 1GHz RISC-V CPU with an input string of 10,000 characters, what is the total runtime for the **inner loop**?

(e) (5 points) What is the speedup of running this program on the RISC V CPU relative to the x86?

2. (10 points) Below I have drawn a gate-level implementation of a 4-to-1 multiplexor. Using the same τ-model that we covered in class, compute the delay through this circuit.



3. (25 points) We are trying to reduce the power consumption of a CPU. The power consumed for the logic blocks in the current design is listed in the table below.

   (a) (10 points) We have come up with a modification of the register file that can reduce its power consumption by 50%. What is the overall reduction in power of the CPU as a whole after modifying the register file?

Logic Block	**Power Consumption**
L1 Inst Cache	1 W
L1 Data Cache	1.5 W
L2 Cache	1 W
Register File	2 W
ALU	1.5W

   (b) (10 points) The improvement made in part a above causes us to have to redesign other components in the CPU, which results in an average increase of cycles per instruction that the CPU can execute. Before the modification, the CPU could execute instructions at a rate of 1.2 cycles per instruction. After the modification, the rate is 1.8 cycles per instruction. Fortunately, the power reduction allows us to clock the CPU at a higher frequency. Before the modification, the clock speed was 1.1 GHz, and after it is 1.5 GHz. **For a fixed program,** which CPU is faster, the one before modification

or the one after?

(c) (5 points) What is the speedup or slowdown after converting to the new design?