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CS 163 Discrete Math
Fall 2019
http://neilklingensmith.com/teaching/loyola/cs163/
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## Half Adder Activity

Date: September 6, 2019

## Name:

1. Fill out the truth table for the half adder.

| $A_{\text {in }}$ | $B_{\text {in }}$ | $C_{\text {in }}$ | $C_{\text {out }}$ | $S_{\text {out }}$ | Sum (Decimal) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 |  |  |  |
| 0 | 1 | 1 |  |  |  |
| 1 | 0 | 0 |  |  |  |
| 1 | 0 | 1 |  |  |  |
| 1 | 1 | 0 |  |  |  |
| 1 | 1 | 1 |  |  |  |

2. Write a boolean logic expression for the following:
$C_{\text {out }}=$
$S_{\text {out }}=$
3. Navigate to https://logic.ly/demo and implement your logic expression with gates. Switches are inputs, and light bulbs are outputs. An example of switches connected
 hrough an AND and OR gate is below
4. When you're finished implementing your half-adder, flag down Neil and demonstrate it. Screen shot your design and save it on your computer. You'll need it for the next lab.
5. If each gate adds 10 ms of delay from input to output, what is the total propogation delay through the circuit? What is the critical path?
